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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leith Johnson
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For:	Virtualized Resources in a Partitionable Server
Examiner:	Sheng Jen Tsai
Art Unit:	2186

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APPELLANTS' BRIEF ON APPEAL

This is an appeal pursuant to 35 U.S.C. § 134 from the Examiner's decision rejecting claims 1-5, 8-11, 14-21, and 28-29 as set forth in the Final Office Action of March 5, 2007.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicant's attorney knows of no related pending appeals or interferences.

STATUS OF CLAIMS

Claims 1-5, 8-11, 14-21, and 28-29 are now pending in this application. Claims 6-7, 12-13, 22-26 and 30-31 are canceled.

Claims 1-5, 8-11, 14-21, and 28-29 stand rejected and are the subject of this appeal. More specifically, claims 1-5, 8-11, 14-21, and 28-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Vishin et al. (U.S. Pat. No. 5,860,146).

Although the Final Office Action states that claims 23, 25, 27, and 30-31 are pending, these claims were canceled by the Response mailed on January 31, 2007, as further clarified by the Response submitted on April 20, 2007, and therefore are not pending. Therefore any references in the Final Office Action to claims 23, 25, 27, and 30-31 are not addressed herein.

STATUS OF AMENDMENTS

An amendment was filed on April 20, 2007 to clarify that claim 23 has been canceled.

SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1-5, 8-11, and 28 all include substantially the same relevant limitations related to creating a physical resource identifier space in a partition of a partitionable computer system. In particular, all of these claims include limitations requiring a mapping that defines a non-monotonic function. The relevance of this limitation will be explained in more detail below.

Table 1 shows the preamble and elements of independent claim 1, and examples of where support for the text of claim 1 may be found in the specification.

Claim Text	Support in Specification
Claim 1. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers,	P. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.

a method for creating a physical resource identifier space in a partition of the partitionable computer system, the method comprising steps of:	FIG. 4; p. 22, line 20 – p. 25, line 3.
establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers,	FIG. 4, steps 406-416; p. 23, line 6 – p. 24, line 8 (the physical-to-machine address translation table is an example of a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers).
wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero,	P. 12, lines 9-10; FIGS. 2A-2B (physical address spaces 202a-b); p. 15, lines 30-32; and p. 17, lines 7-11, 22-28.
and wherein the mapping defines a non-monotonic function; and	FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).

(B) providing, to an operating system executing in the partition, an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers.	FIGS. 2A-2B (the virtual-to-physical translation mechanisms 204a-b are examples of interfaces to operating systems); p. 15, line 33 - p. 16, line 14.

Table 1: Claim 1

Independent claim 8 contains substantially similar limitations, which find support in at least the same places in the specification. More specifically, Table 2 shows the preamble and elements of independent claim 8, and examples of where support for the text of claim 8 may be found in the specification.

Claim Text	Support in Specification
Claim 8. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, an apparatus comprising:	P. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.

mapping means for establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers,	FIG. 4, steps 406-416; p. 23, line 6 – p. 24, line 8 (the physical-to-machine address translation table is an example of a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers).
wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero,	P. 12, lines 9-10; FIGS. 2A-2B (physical address spaces 202a-b); p. 15, lines 30-32; and p. 17, lines 7-11, 22-28.
and wherein the mapping defines a non-monotonic function; and	FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).
interface means for accessing the at least some of the plurality of machine resources in response to requests from an operating system executing in a partition of the partitionable computer system, wherein the requests identify the at least some of the plurality of machine resources using the plurality of physical resource identifiers.	FIGS. 2A-2B (the virtual-to-physical translation mechanisms 204a-b are examples of interfaces to operating systems); p. 15, line 33 – p. 16, line 14.

Table 2: Claim 8

Claims 14-21 and 29 all include substantially the same relevant limitations related to accessing a physical machine resource in a partitionable computer system. In particular, all of these claims include limitations requiring a mapping that defines a non-monotonic function. Table 3 shows the preamble and elements of independent claim 14, and examples of where support for the text of claim 14 may be found in the specification.

Claim Text	Support in Specification
Claim 14. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers,	P. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.
a method for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the method comprising steps of:	FIG. 5; p. 25, line 3 - p. 26, line 9.
(A) identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality	FIG. 5, element 504; p. 25, lines 27-29; and FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).

of machine resource identifiers, and wherein the mapping defines a non-monotonic function;	
(B) translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and	FIG. 5, element 506; p. 25, lines 29-32.
(C) causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.	FIG. 5, element 508; p. 25, line 32 - p. 26, line 2.

Table 3: Claim 14

Independent claim 18 contains substantially similar limitations, which find support in at least the same places in the specification. More specifically, Table 4 shows the preamble and elements of independent claim 18, and examples of where support for the text of claim 18 may be found in the specification.

Claim Text	Support in Specification
Claim 18. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers,	P. 12, lines 18-31; FIGS. 3A-3B (showing examples of machine resources); p. 13, line 20 - p. 15, line 23); FIG. 2C (machine memory blocks 210a-e); p. 16, lines 15-31 (machine addresses 216 are examples of "machine resource identifiers"); and FIGS. 6A-6B (machine resource identifiers 616a-g); p. 36, line 9 - p. 37, line 3.
an apparatus for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the apparatus comprising:	FIG. 5; p. 25, line 3 - p. 26, line 9.

means for identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;	FIG. 5, element 504; p. 25, lines 27-29; and FIGS. 2A-2C (e.g., mapping between physical addresses 218a and the corresponding portion of machine addresses 216).
means for translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and	FIG. 5, element 506; p. 25, lines 29-32.
means for causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.	FIG. 5, element 508; p. 25, line 32 - p. 26, line 2.

Table 4: Claim 18

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The single ground of rejection for review is the rejection of claims 1-5, 8-11, 14-21, and 28-29 under 35 U.S.C. § 102(b) as being anticipated by Vishin et al. (U.S. Pat. No. 5,860,146).

ARGUMENT

Rejection of Claims 1-5, 8-11, 14-21, 23, 25, and 28-29 under 35 U.S.C. § 102(b) (Vishin)

Claims 1-5, 8-11, 14-21, and 28-29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Vishin et al. (U.S. Pat. No. 5,860,146).

Vishin does not, however, disclose "providing, to an operating system . . ., an interface for the operating system to access . . the plurality of machine resources using the plurality of physical resource identifiers," as expressly recited by claim 1. Vishin fails to disclose an express element of claim 1. Claim 1, therefore, patentably distinguishes over Vishin.

In general, Vishin discloses a system for "translating virtual addresses into physical addresses" (Abstract). Assume solely for purposes of argument that the "physical resource identifiers" of claim 1 read on the "virtual addresses" of Vishin, and that the "machine resource identifiers" of claim 1 read on the "physical addresses" of Vishin. As a result, assume solely for purposes of argument that the physical-to-machine mapping recited in step (A) of claim 1 reads on the virtual-to-physical translation disclosed by Vishin.

Even given this assumption, Vishin does not disclose step (B) of claim 1, namely "providing, to an operating system . . ., an interface for the operating system to access . . the plurality of machine resources using the plurality of physical resource identifiers." The specification of the present application provides examples of step (B). For example, the specification discloses that the memory model 200 of FIG. 2 includes a physical-to-machine translation mechanism 210 for transparently performing a translation between physical addresses in a physical address space 202a and machine addresses 216 in a machine address space 202. (Specification, at p. 16, line 32 - p. 17, line 11). The physical-to-machine translation mechanism 210 is an example of the interface recited in claim 1.

For example, the specification further states that when a process (such as an operation system 324a) executing in partition 322a (FIG. 3) attempts to *access* a memory location using a physical address in the physical address space 202a, the physical address is first translated (by the physical-to-machine translation mechanism 210) into a machine (hardware) memory address before the *memory access* occurs. (Specification, at p. 16, line 32 - p. 17, line 11). This is an example of "providing, to an operating system . . ., an interface for the operating system to *access* . . the plurality of machine resources using the plurality of physical resource identifiers" (emphasis added), as expressly recited in claim 1.

Examples of memory "access" requests include requests to write to memory and requests to read from memory. (See, e.g., p. 24, line 31 - p. 25, line 3).

Vishin, in contrast, does not disclose that the operating system *accesses* machine resources ("physical" resources in Vishin's terms) by referencing such resources using physical resource identifiers ("virtual" resources in Vishin's terms). Although the Office Action points to col. 5, lines 33-59 of Vishin, this passage merely states that remote translation lookaside buffer (RTLB) 160 is organized into groups of entries, and that "it is the responsibility of the operating system 180 . . . to make sure that the RPTEs in different groups do not have overlapping address ranges." The fact that the operating system 180 manages the organization of the contents of the RTLB does not indicate or imply that the operating system itself accesses machine resources ("physical" resources in Vishin's terms) using physical resource identifiers ("virtual" resources in Vishin's terms), and Vishin does not disclose any "interface" that is provided to the operating system for doing so. Vishin does not disclose, for example, that the operating system 180 attempts to read from or write to memory by referencing such memory using virtual addresses, and that an interface translates such references into physical addresses.

In fact, Vishin discloses that *application programs*, not the operating system 160, access memory locations using virtual addresses, which are translated into physical addresses. (See, for example, Vishin at col. 1, lines 39-40; col. 3, lines 47-61).

In summary, Vishin fails to disclose an express element of claim 1, namely, "providing, to an operating system . . ., an interface for the operating system to access . . . the plurality of machine resources using the plurality of physical resource identifiers." Claim 1, therefore, patentably distinguishes over Vishin.

Although the Final Office Action asserts generally that Vishin anticipates the express limitations of claim 1 described above, the Office Action does not point out any portion of Vishin which describes enabling the operating system to access machine resources *using a plurality of physical resource identifiers* having the features recited in claim 1. Instead, the Office Action relies on two teachings of Vishin, neither of which anticipates the express limitations of claim 1 described above. First, the Office Action states that:

> Vishin teaches that "In response to the page fault the operating system of the cluster 102 will request the memory controller 112 to retrieve the specified page from secondary

> memory 110 and store it in a free page in primary memory 108" (column 2, lines 36-40). Thus, it is clear that an interface is provided to the operating system to access the memory controller, which is part of the machine resources, to retrieve the specified page from secondary memory 110 and store it in a free page in primary memory 108. (Office Action, p.2.)

Note that the Office Action merely points out that Vishin describes an interface for the operating system to access the memory control, but does not even allege that Vishin describes an interface for the operating system to access memory *using a plurality of physical resource identifiers* having the specific express features recited in claim 1. The Office Action, by failing to acknowledge an express limitation of claim 1, fails to make out even a *prima facie* case of anticipation.

Similarly, the Office Action states that:

> Vishin teaches that "it is the responsibility of the operating system 180 (see FIG. 9) to make sure that the RPTEs in different groups do not have overlapping address ranges" (column 5, lines 33-59). Thus it is clear that an interface is provided to the operating system to

> access the RPTEs (Remote Page Table Entries), which is also part of the machine resources, to make sure that the RPTEs in different groups do not have overlapping address ranges. (Office Action, pp.2-3.)

Note again that the Office Action merely points out that Vishin describes providing an interface to access machine resources, but does not even allege that Vishin describes an interface for the operating system to access these resources *using a plurality of physical resource identifiers* having the specific express features recited in claim 1. Again, by failing to acknowledge an express limitation of claim 1, the Office Action fails to make out even a *prima facie* case of anticipation.

Furthermore, the Office Action's allegation that the Applicant has argued limitations which are not claimed (Office Action, p.3) is incorrect. The Applicant has not, either in any Response or in this Appeal Brief, argued any limitations which are not claimed. Instead, the Applicant has pointed to the specification for illustrative *examples* of particular claim limitations in order to aid in the understanding of those claim limitations. None of Applicant's arguments rely on limitations which are not claimed.

For at least the reasons provided above, claim 1 patentably distinguishes over Vishin. Applicant therefore requests that the rejection of claim 1 be reversed.

Claims 2-5 depend from claim 1 and therefore patentably distinguish over Vishin for at least the same reasons.

Claim 8 includes substantially the same relevant limitations as claim 1 and therefore patentably distinguishes over Vishin for at least the same reasons. Claims 9-11 and 28 depend from claim 8 and therefore patentably distinguish over Vishin for at least the same reasons.

Claims 14 and 18 include substantially the same relevant limitations as claim 1 and therefore patentably distinguish over Vishin for at least the same reasons. Claims 15-17, 19-21, and 29 depend from claims 14 and 18, respectively, and therefore patentably distinguish over Vishin for at least the same reasons.

CONCLUSIONS

The Examiner's rejections of claims 1-5, 8-11, 14-21, and 28-29 should be reversed for the reasons stated above.

If this Brief is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 08-2025.

Respectfully submitted,

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APPENDIX A: CLAIMS ON APPEAL

Claim 1. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, a method for creating a physical resource identifier space in a partition of the partitionable computer system, the method comprising steps of:

(A) establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers, wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero, and wherein the mapping defines a non-monotonic function; and

(B) providing, to an operating system executing in the partition, an interface for the operating system to access the at least some of the plurality of machine resources using the plurality of physical resource identifiers.

Claim 2. The method of claim 1, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 3. The method of claim 1, further comprising a step of performing the steps (A) and (B) for each of a plurality of partitions of the partitionable computer.

Claim 4. The method of claim 1, wherein the step (A) comprises a step of creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers.

Claim 5. The method of claim 1, wherein the interface comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping.

Claim 8. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, an apparatus comprising:

mapping means for establishing a mapping between a plurality of physical resource identifiers and at least some of the plurality of machine resource identifiers, wherein the plurality of physical resource identifiers are numbered sequentially beginning with zero, and wherein the mapping defines a non-monotonic function; and

interface means for accessing the at least some of the plurality of machine resources in response to requests from an operating system executing in a partition of the partitionable computer system, wherein the requests identify the at least some of the plurality of machine resources using the plurality of physical resource identifiers.

Claim 9. The apparatus of claim 8, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 10. The apparatus of claim 8, wherein the mapping means comprises means for creating an address translation table that records the mapping between the plurality of physical resource identifiers and the at least some of the plurality of machine resource identifiers.

Claim 11. The apparatus of claim 8, wherein the interface means comprises means for translating a physical resource identifier selected from among the plurality of physical resource identifiers into one of the plurality of machine resource identifiers in accordance with the mapping.

Claim 14. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, a method for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the method comprising steps of:

(A) identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;

(B) translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and

(C) causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.

Claim 15. The method of claim 14, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 16. The method of claim 14, wherein the step (C) comprises a step of reading a datum from the machine memory address.

Claim 17. The method of claim 14, wherein the step (C) comprises a step of writing a datum to the machine memory address.

Claim 18. In a partitionable computer system including a plurality of machine resources having a plurality of machine resource identifiers, an apparatus for accessing a select one of the plurality of machine resources specified by a physical resource identifier provided by an operating system executing in a partition in the partitionable computer system, the apparatus comprising:

means for identifying a mapping associated with the partition, wherein the mapping maps a plurality of physical resource identifiers in a sequential zero-based physical resource identifier space of the partition to at least some of the plurality of machine resource identifiers, and wherein the mapping defines a non-monotonic function;

means for translating the physical resource identifier into a machine resource identifier using the mapping, wherein the machine resource identifier specifies the select one of the plurality of machine resources; and

means for causing the select one of the plurality of machine resources to be accessed using the machine resource identifier.

Claim 19. The apparatus of claim 18, wherein the plurality of machine resources comprises a plurality of machine memory locations, wherein the plurality of machine resource identifiers comprises a plurality of machine memory addresses, and wherein the plurality of physical resource identifiers comprises a plurality of physical memory addresses.

Claim 20. The apparatus of claim 18, wherein the means for accessing comprises means for reading a datum from the machine memory address.

Claim 21. The apparatus of claim 18, wherein the means for accessing comprises a means for writing a datum to the machine memory address.

Claim 28. The method of claim 8, wherein the interface means comprises a Content Addressable Memory that establishes the mapping.

Claim 29. The method of claim 18, wherein the means for translating comprises a Content Addressable Memory.

APPENDIX B: EVIDENCE

No evidence is submitted in support of this Appeal Brief.

APPENDIX C: RELATED PROCEEDINGS

Applicant's attorney knows of no related pending appeals or interferences.